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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,244	10/20/2003	Andrew Spencer	10014282-1	3876

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EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

MAIL DATE	DELIVERY MODE
10/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,244	SPENCER, ANDREW	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-20 and 24-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-20 and 24-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4-20 and 24-36 are presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. The rejections are respectfully maintained and incorporated by reference to the extent that is applicable to the newly amended claims as set forth in the last office action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 2 and 4-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As to claim 1, the newly added limitation "by determining a number of times that buffer is full and empty from the at least one signal over a time period"" is not described in the specification.

Claims 2 and 4-9 are rejected because they incorporate the deficiencies of claim 1.

6. Claims 10-18 and 28-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aizawa (Aizawa), U.S. patent no. 6,407,941 in view of Trost (Trost), US patent no. 4,288,860.

As per claim 10, Aizawa discloses a system [fig. 1] comprising:

a host device [12, fig. 1]; and a memory card configured to couple to the host device [fig. 1]; wherein the memory card includes a storage media, wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate [fig. 1; col. 5, lines 30-34, 48-49].

Aizawa does not explicitly disclose that the memory card is configured to count a number of transaction received by the memory care from the host device during a time period, generating a clock signal at a clock rate varies in dependence on a number of transactions received by the memory card from the host device during a time period.

Trost discloses that the memory card is configured to count a number of transaction received by the memory care from the host device during a time period [col. 4, lines 18-37, 58-65; fig. 2], generating a clock signal at a clock rate varies in dependence on a number of transactions received by the memory card from the host device during a time period [fig. 1; abstract all; col. 2, lines 3-34; col. 3, line 56-col. 4, line 16; col. 7, line 65-col. 8, line 10].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Aizawa and Trost, because they both disclose a data storage system, the specify teachings of Trost stated above would improve the

performance of Aizawa system adjusting the clock signal corresponding a data transmission rate to reduce power consumption of the memory card.

As per claim 11, Aizawa discloses that the memory card includes a processor system and a control circuit coupled to the processor system [fig. 1; col. 3, lines 14-26]. Trost discloses that the processor system is configured to count the number of transactions received by the memory card from the host device during the time period, and wherein the processor system is configured to cause the control circuit to set the rate of the first clock signal in response to the number of transactions [col. 4, lines 18-37, 58-65].

As per claim 12, Aizawa discloses that the memory card includes a buffer and a buffer management circuit [col. 3, lines 14-26]. Trost discloses that the buffer management circuit is configured to provide information to the processor system, and wherein the processor system is configured to count the number of transactions received by the memory card during the time period using the information [col. 4, lines 18-37, 58-65].

As per claim 13, Trost discloses a clock configured to provide a second clock signal to the processor system and the control circuit at a second clock rate, and wherein the control circuit is configured to generate the first clock signal using the second clock signal [fig. 1; col. 2, lines 3-34; col. 3, line 56-col. 4, line 16; col. 7, line 65-col. 8, line 10].

As per claim 14, Aizawa discloses that host device comprises a digital camera [col. 3, lines 9-10].

As per claim 15, Aizawa discloses that the memory card includes a buffer and an interface coupled to the buffer, and wherein the interface is coupled to receive the transactions from the host device and provide the transactions to the buffer [col. 3, lines 14-20].

As per claim 16, Aizawa discloses that the transactions include read transactions configured to cause information to be read from the memory card and provided to the host device [col. 3, lines 19-20; col. 4, lines 23-37].

As per claim 17, Aizawa discloses that the transactions include write transactions configured to cause information to be written from the host device to the memory card [col. 3, lines 19-20; col. 4, lines 23-37].

As per claim 18, Aizawa discloses that the transactions include read transactions configured to cause first information to be read from the storage media and provided to the host device and write transactions configured to cause second information to be written from the host device to the memory card [col. 3, lines 19-20; col. 4, lines 23-37].

Regarding to claims 28-36 are written in mean plus functions and contained the same limitations as claims 10-18. Therefore, same rejection is applied.

7. Claims 19, 20 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aizawa (Aizawa), U.S. patent no. 6,407,941 in view of Trost (Trost), US patent no. 4,288,860 and Sherburne, Jr. (Sherburne), U.S. patent no. 6,990,598[1].

[1] Sherburne is cited in prior office action.

Regarding to claims 19, 20 and 24-27, Aizawa and Trost together teaches the limitations of claimed system for carrying out the method of steps of claims 19, 20 and 24-27.

Aizawa and Trost do not explicitly disclose that determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level.

Sherburne discloses that determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level [col. 3, lines 8-23; col. 7, lines 6-13; col. 8, lines 30-37].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Aizawa and Trost and Sherburne, because they disclose a data system, the specify teachings of Sherburne stated above would improve the performance of Aizawa system adjusting the clock signal corresponding a data transmission rate by comparing buffer level to a threshold level.

Therefore, Aizawa and Trost and Sherburne teach the limitations of claimed system for carrying out the method of steps of claims 19, 20 and 24-27.

Response to Arguments

8. Applicant's arguments filed on 8/13/2007 have been fully considered but are moot in view of new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oct. 19, 2007

CHUN CAO
PRIMARY EXAMINER